REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (*Leave Blank*)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
		Final report: 08/19/2002 thru 06/19/2003

4. TITLE AND SUBTITLE
Large Area Substrates for InP Based Electronics and Optical Device Manufacturing

5. FUNDING NUMBERS

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7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
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8. PERFORMING ORGANIZATION REPORT NUMBER
Final

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
U.S. Army Space Missile Defense Command
P.O. Box 1500
Huntsville, AL 35807-3801

10. SPONSORING / MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION / AVAILABILITY STATEMENT
Approved for Public Release; Distribution Unlimited

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

InP-based materials enable optoelectronic and high speed devices. InP structures are limited in a real size, which greatly adds to the cost of InP devices. Conversely, silicon wafers are an order of magnitude larger and less costly. This STTR program seeks to create device quality InP layers on silicon substrates. The lattice mismatch between Si and InP would normally create defects in the crystal and result in poor material quality. To achieve good InP growth, a thin oxide buffer layer is grown on top of the Si prior to the InP. This oxide layer absorbs the strain mismatch between the two materials. The Phase I has demonstrated InP on Silicon with good structural and optical quality. Optimization of the process will be conducted in Phase II. At the conclusion of the Phase II, a prototype

14. SUBJECT TERMS	15. NUMBER OF PAGES
STTR Report	28
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	UL

NSN 7540-01-280-5500

Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. Z39-1

Large Area Si Substrates for InP Based Electronics and Optical Device Manufacturing

Contract: DASG60-02-p-0276

Final Report

Technical Monitor: Latika Becker
MDA

Submitted by
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June 18, 2003

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1. Summary of Project Results

This Phase-I STTR program investigated the technology to create economical large area InP substrates. The method to accomplish this was to epitaxially grow InP thin films on silicon wafers. Silicon was chosen because it is fairly inexpensive and is available in wafer sizes greater than 12 inches diameter. The obstacle to obtaining good quality InP on Si is the inherent lattice mismatch between the two crystal structures. To solve this problem, the material strontium titanate ($SrTO_3$, a.k.a. STO) was chosen to serve as an interface to allow the growth of III-V semiconductors, such as InP, on silicon.

Northwestern University is a partner in this research program. Their group has particular expertise in growing thin film oxides, such as STO. For this study, the deposition and formation of STO on Si was extensively performed and studied. STO layers were analyzed using reflection high energy electron diffraction (RHEED), x-ray diffraction and atomic force microscopy (AFM). High quality STO films on Si were achieved. These films were then utilized in the second thrust of this program.

Solid source molecular beam epitaxy (MBE) was employed at SVT Associates to grow layers of III-V compound semiconductor films, including InP and GaAs. InP was epitaxially grown on various oxide/silicon combinations, such as magnesium oxide (MgO), silicon-on-insulator (SOI) and STO. Intermediate buffer layers were used to accommodate the lattice and thermal mismatch to improve the final InP film. The effects of buffer layers were examined, comparing the InP quality versus the type of buffer, such as GaAs and GaP. Final growths of InP were performed on the STO on Si samples produced by Northwestern.

The results of this Phase-I study proved the viability of growing high quality single crystal InP on silicon wafers using an STO interfacial layer. This InP layer was found to be of high quality structurally based on x-ray data, optically based on photoluminescence spectra and electrically based on Van Der Pau measurements. These results justify a continuation of this research into the Phase II.

The major accomplishments:

- **High quality oxide templates have been demonstrated**
- **Several compliant buffer layers have been investigated for subsequent InP growth**
- **Epitaxial InP layers have exhibited excellent structural and optical quality**

2. Introduction

The goal of this program is to develop an enabling technology for low cost InP device manufacturing. InP devices have both commercial and military applications encompassing the entire communication technology including wireless and fiber-optic communications. They are especially important for high frequency (> 200 GHz) applications. Their manufacturing costs have remained high in large part due to the high cost and the relatively small available InP substrates. Device throughput per wafer is proportional to the square of the wafer diameter, so to gain economy of scale the growth of InP on larger wafers offers a significant economic advantage. To accomplish this we are developing an epitaxial process for the deposition of InP on Si using oxide buffer layer technology.

Compound semiconductor micro- and opto-electronics are becoming increasingly important in all military missions. InP-based materials offer significant performance advantages compared to GaAs. By InP-based materials we refer to a broad class of materials that are closely lattice matched to InP substrates including InGaAs, InAlAs, InAlGaP and GaAsSb.

InP-based devices have demonstrated frequency performance as high as 300 GHz, and have enabled numerous millimeter-wave applications like satellite crosslinks, up and down links, point-to-point systems, local multipoint distribution systems and so on. They spur broad applications such as scientific instruments, earth observation, passive millimeter-wave imaging and automotive radar. Many of these areas have obvious military implications.

Until now, both the military and industry have been dependent on costly GaAs and InP wafers for high performance optical and high-frequency applications. Because of their brittle nature, no one has previously been able to create commercial GaAs wafers larger than 150 mm, or InP wafers larger than 100 mm. By comparison in silicon industry 300 mm diameter wafers are already production standard. In addition to the substrate cost, a more important factor is the device output per wafer which is proportional to the square of wafer diameter. Hence to gain economy of scale large wafer size is much more favorable. Furthermore, system performance may benefit from integration of the semiconductor devices directly on silicon. Examples are laser with driver electronics and imaging detector with read-out electronics; novel concepts such as optical interconnect may also be realized.

In this Phase I project we endeavored to investigate the formation of III-V compound materials on silicon through engineered oxide interfaces. Although there have been many attempts to grow GaAs on silicon, only limited success has been achieved in the past. This is due to lattice and thermal mismatch, and antiphase domain formation. As pioneered by Motorola two years ago, these difficulties can be in large part overcome by using suitable oxide buffer layer to provide better lattice match as well as material compliancy to accommodate the resulting strain. The latter is especially crucial in preventing strain induced (thermal and lattice mismatch) defect generation in the grown layers. There are a large number of oxide compounds available, and we began the project by selecting candidate materials for the buffer growth.

In Figure 2.1 a compilation of the lattice constants of various semiconductor compounds of important opto- and micro-electronic interest, and their comparison with the available Perovskite

compounds. In particular, a combination of $(Sr,Ba)ZrO_3$, $BaSnO_3$, $Ba(Ti,Zr)O_3$, $(Sr,Ba)SnO_3$ and $Sr(Ti,Zr)O_3$ can be lattice matched to InP-based materials. In this work we deposited these candidate oxides on Si substrates either directly or through intermediate buffers such as MgO. InP growth was then performed on these buffer layers to check the material quality.

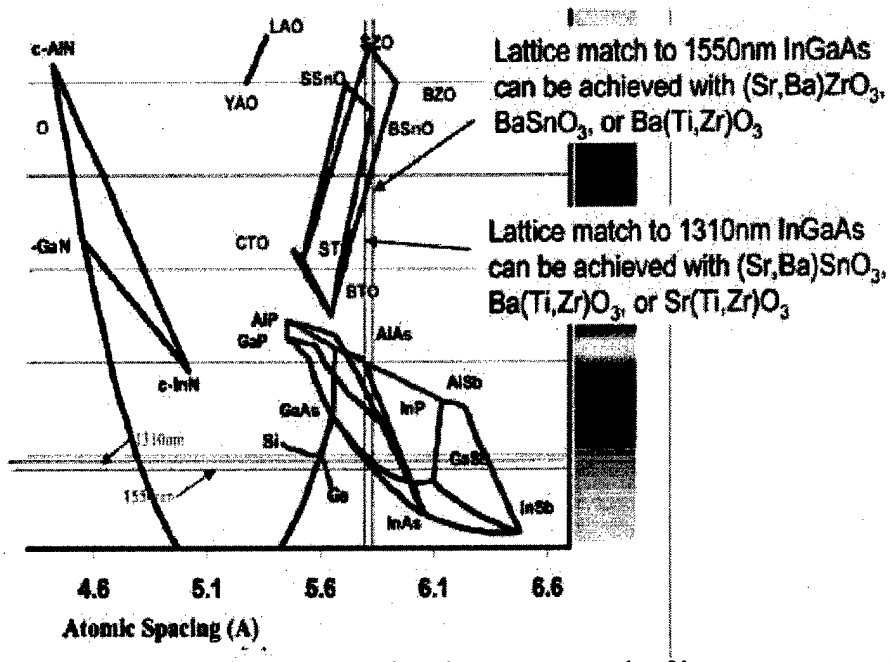


Figure 2.1. Lattices of various III-V semiconductor compounds of important opto- and micro-electronic interest, and how they compare with the available Peroskite compounds (W.J. Ooms, Motorola).

For this program we focused the effort on the material strontium titanate (STO) which has a structure classified as Perovskites. STO is a material with a high dielectric constant (high k) that has applications as a gate dielectric and for DRAM capacitors. Strontium titanate has a lattice which is about 2% mismatched to silicon, about halfway between silicon and gallium arsenide. Interestingly, it was found that there is an interface layer between the STO and the silicon, which was an amorphous silicon dioxide. From early SiGe work at IBM it has been known that amorphous silicon dioxide can act as a compliant layer. When looking at the crystalline structure of the strontium titanate, it was completely relaxed. This layer then can serve a buffer layer for growth of other material.

Subsequently GaAs and InP were grown on this STO buffer layer. In this STTR program SVTA collaborated with Professor Bruce Wessels's group at Northwestern University. They have spent a significant amount of effort to grow single crystal STO which was than sent to SVTA as template for GaAs and InP deposition.

3. Oxide Growth on Si

High quality epitaxial $SrTiO_3$ (STO) as a template for integration of epitaxial III-V compound semiconductor, i.e., GaAs, on Si has been successfully demonstrated by Motorola in 2001. 12" GaAs on Si wafer has been fabricated using production-type MBE. A mobility of 2524 cm^2/V-s for GaAs/STO/Si was reported as compared with 2682 cm^2/V-s for GaAs/GaAs, which greatly encourages the effort to growing other III-V materials on Si substrate. In the pursuit of growing InP on Si as proposed in this STTR project, epitaxial STO has been developed on Si as a buffer layer for InP overgrowth. This part of research is carried out in Prof. Bruce Wessels' group at Northwestern University. Main research efforts and accomplishments are reported as follows:

Growth precedure of STO on Si

Epitaxial growth of STO on Si has been performed in an ultra-high vacuum MBE system developed by SVT Associates. The MBE system was modified to enable evaporation of refractory metals and complex oxides. A high temperature effusion cell (up to 2000?C), designed and provided by SVTA has been shown to work successfully for growing transition metal oxides by MBE.

The base pressure of the MBE system is typically around 10^{-9} to 10^{-10} Torr. Ti elemental source with a purity of 99.999% (metal based) was loaded in a tungsten crucible and high temperature effusion cell provided by SVTA. Elemental Sr with a purity of 98+% (metal basis) and Mg with a purity of 99.98 (metal basis) were loaded into PBN effusion cells and used as evaporation sources. High purity molecular O_2 gas (grade 4.8) was used as oxidant source. Phosphorus doped n-type silicon (001) wafers with a resistivity of 1.0-10.0 ohm-cm and 3 inches in diameter were used as substrates. An in–situ Reflection High-Energy Electron Diffraction (RHEED) gun with an electron beam voltage of 10kV was used for monitoring surface structures of thin films.

To form a template, a 0.5 ML Sr silicide layer was usually deposited first at 700?C on clean Si wafers to passivate and stabilize the Si surfaces. A clean Sr/Si(2?1) RHEED pattern should be observed after this deposition.

Two methods of epitaxial STO depoistion were pursued:

1. direct co-deposition of Sr and Ti at a substrate temperature of 700°C;
2. codeposition of amorphous STO at 200°C and subsequent recrystallization at 600-700°C.

To optimize STO growth temperature, O_2 partial pressure and most importantly, Sr/Ti flux ratio were varied to obtain the right STO stoichiometry.

Besides in-situ RHEED, XRD ?-2? scan and rocking curves were measured with a diffractometer specially set up for measuring very thin epitaxial films. Secondary ion mass spectroscopy (SIMS) and x-ray photoelectron spectroscopy (XPS) was used to measure Sr and Ti composition. AFM was used to analyze STO surface morphology.

The detailed results from these two methods are given as follows:

One step co-deposition at 700? C

1. Optimizing deposition temperature:

Figure 3.1 shows RHEED patterns from STO films deposited at different substrate temperatures. The intial Sr/Ti flux ratio was estimated according to the measured metal deposition rate. O_2 partial pressure was kept in excess during STO growth at 8.0?10^{-8} Torr. Lower O_2 pressure (=2.0?10^{-8} Torr) usually produced poorer film crystallinity. At 400?C, a polycrystalline film was obtained, while at 550? a textured film was obtained. Film deposited at 700?C showed a single crystal RHEED pattern even though extra spots associated with multiple phases and non stoichiometric Sr/Ti ratio are also present. This has been confirmed by XPS analysis (not shown here), which indicated a Ti deficient film. Refractive index of the film(#3) measured by ellipsometry also gave a lower value of 1.6 compared to bulk value of 2.38,which indicated a SrO rich film composition.

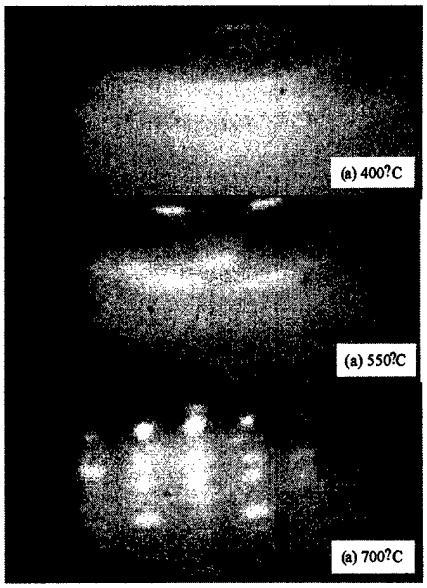


Fig 3.1. RHEED patterns from STO films deposited at different substrate temperatures.

2. Optimizing of Sr/Ti composition(stoichiometry) by RHEED.

Based on the XPS and ellipsometry results it was concluded that a higher Ti flux was required, we have decreased the Sr/Ti flux ratio by increasing the Ti source temperature and reducing Sr source temperatures. Figure 3.2 shows RHEED patterns of STO films deposited at different Sr/Ti flux ratios. All the films were deposited at a substrate temperature of 700?C and an O_2 partial pressure of 8?10^{-8} Torr. So far the growth with a Sr/Ti flux ratio of 0.75 gave the best result with one dominant single phase. The optimal Sr source temperature was at 375±10°C when the Ti source temperature was held constant at 1397°C.

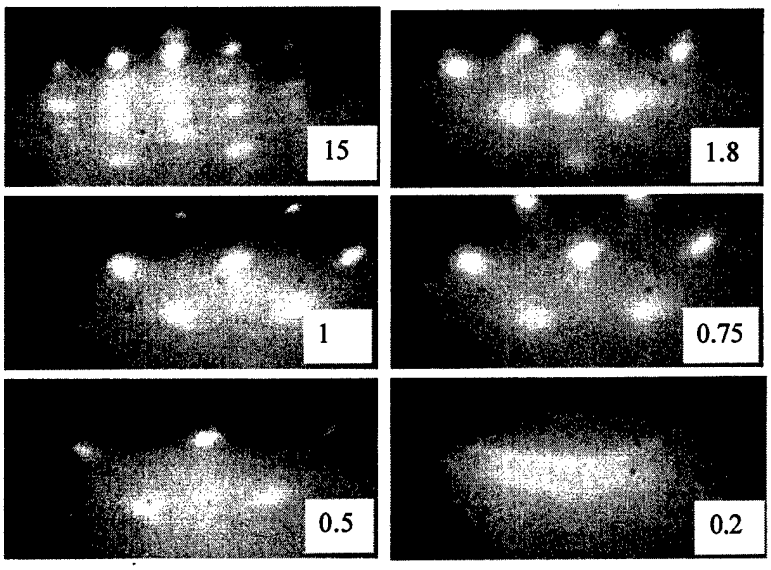


Fig. 3.2. RHEED patterns from STO films deposited at different Sr/Ti flux ratios from 15 to 0.2. The e-beam was along <100> Si.

3. Characterization of STO film

RHEED: The RHEED pattern indicated that a single crystalline, single phase, epitaxial film was deposited. The lattice parameters of the STO film was calculated based on RHEED pattern using either known MgO or SrO or Si substrates as standards, which gives a lattice constant (=3.92 Å) close to bulk STO lattice constant (=3.91Å) within 2% error. The epitaxial relation between STO and underlying Si substrates is STO(001)//Si(001), and STO[100]//Si[110]. RHEED patterns were very spotty indicating a rough, 3D surface morphology. The angular distribution of intensity in the diffraction spots indicates a mosaic spread of misorientation. In addition, the directly co-deposited film usually had high diffuse background level in the RHEED, presumably due to formation of amorphous SiO_x underneath STO film.

XRD results: Figure 3.3 shows an XRD ?-2? scan from the STO/Si, the STO (002) peak was observed, which is parallel to the Si(004) peak. A Si(002) peak and a unidentified peak were also observed.

SIMS:SIMS spectrum from the STO film with a Sr/Ti flux ratio of 1 showed that the film was still Sr rich compared to spectrum from a STO standard sample, even though RHEED pattern showed the STO phase was predominant. Sr source temperature was thus decreased to 375°C for all the films deposited later(#7 and above).

AFM: Figure 3.4 showed AFM images from STO films grown with Sr/Ti flux ratios of 1 and 0.75, respectively. They both have similar columnar morphology with an average size of 100-200 nm, the surface RMS roughness were 3.2 nm and 6.6 nm respectively.

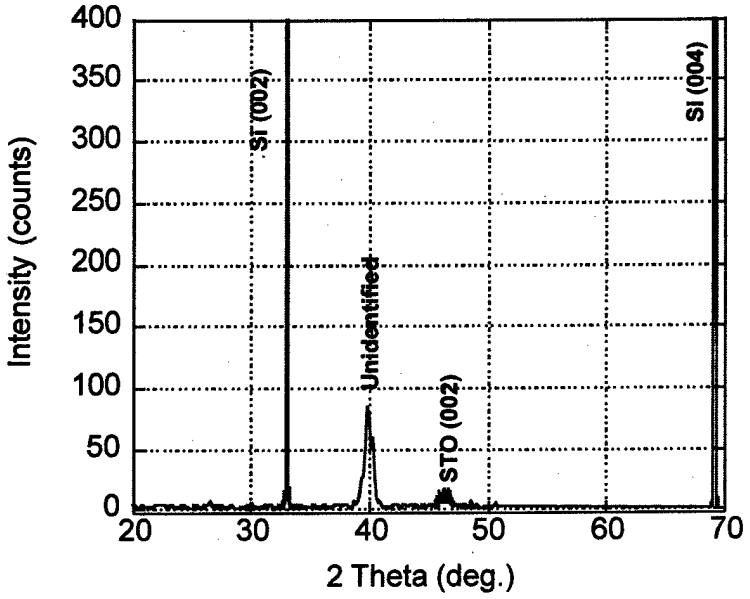


Fig. 3.3. XRD ?-2? scan from a STO/Si sample.

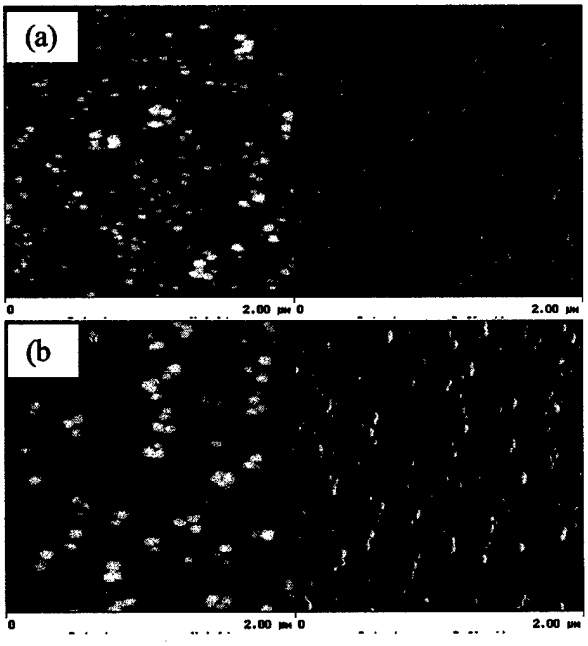


Fig. 3.4. AFM morphology from STO films grown with Sr/Ti flux ratios of (a) 1 and (b) 0.75. The size of all scans are 2?m by 2?m. The RMS roughness were 3.2 nm and 6.6 nm, respectively.

Thickness dependence of structure: Figure 3.5 revealed an evolution of RHEED pattern during STO growth. STO deposit showed a uniform background in the first 10 minutes, then a single crystal RHEED pattern developed from 10-30 minutes. This transformed into a different pattern after further growth. The two crystal patterns have same lattice positions except that every other spots disappear.

4. MgO/STO heterostructures

In order to prove that STO is a suitable template platform for subsequent epitaxial growth of III-V semiconductors, epitaxial growth process for MgO on STO buffered Si by MBE was developed. It was found that crystallinity of MgO layer depended on STO thickness. Poly-MgO was obtained when the STO layer was thin(= 6nm). Figure 3.6 shows a RHEED pattern from a MgO film deposited on 15 nm thick STO, epitaxial MgO was successfully obtained. Figure 3.7 shows an AFM image from the MgO/STO/Si sample. The sample surface is fairly smooth with a RMS roughness less than 2 nm. This experiment demonstrated that STO is an excellent template layer.

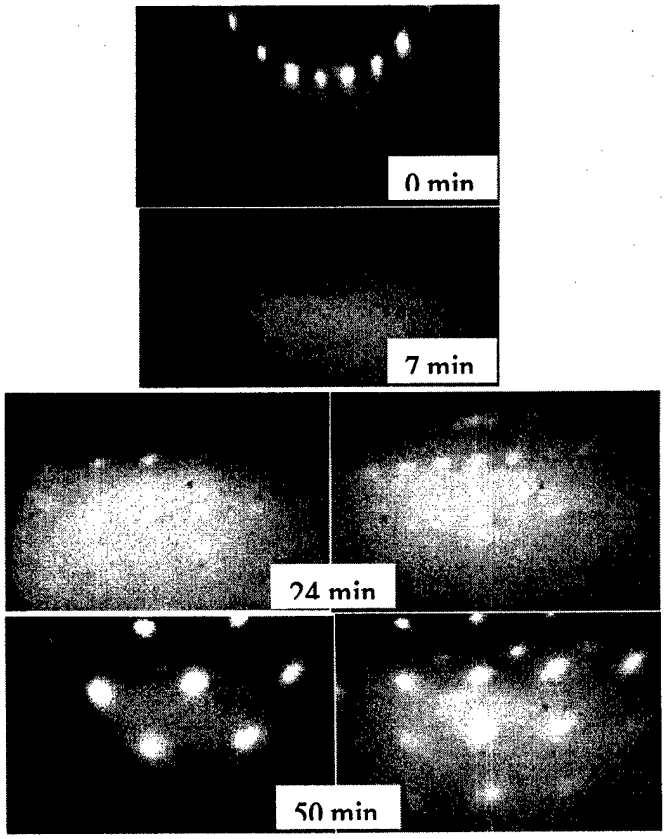


Fig. 3.5. Evolution of RHEED patterns during direct co-deposition of STO on Si at 700?C.

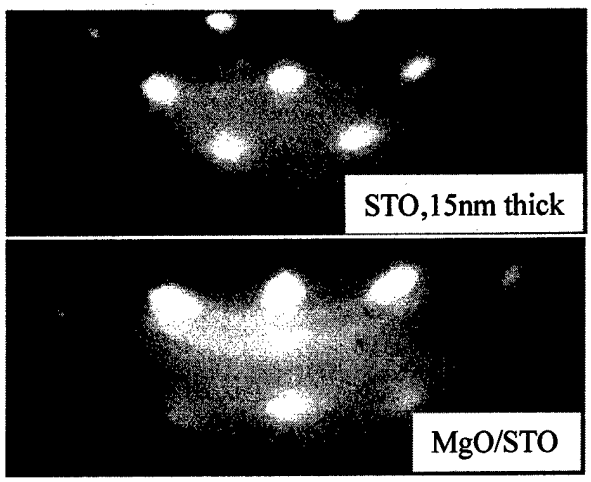


Fig. 3.6. RHEED patterns from MgO on STO/Si.

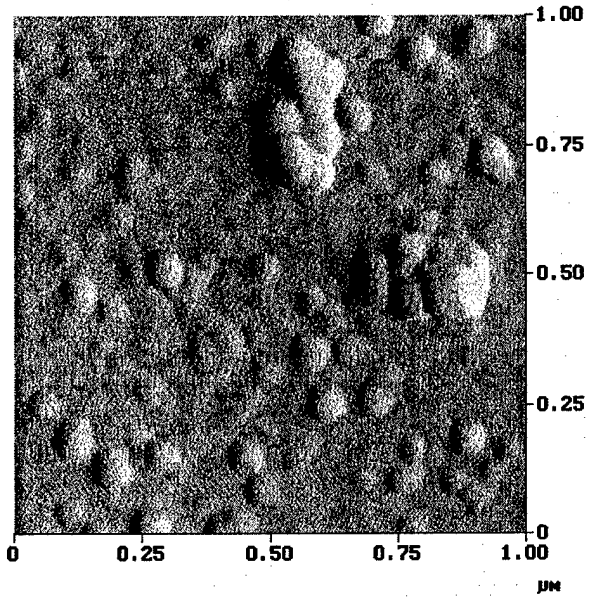


Fig. 3.7. AFM image taken from the MgO/STO/Si sample.

Multi-step recrystallization process

Epitaxial growth of STO was also developed using the solid state epitaxy method. In this case several monolayers of STO was first deposited at 200°C on the $SrSi_2$ stabilized surface with a Sr/Ti flux ratios of 0.75. The STO was ramped up to 600-700° C for recrystallization in vacuum (without additional O_2). The two step cycle was repeated until desired STO layer thickness was reached. Figure 3.8 shows the evolution of RHEED patterns for the first 3ML deposition and subsequent recrystallization. Amorphous

STO was usually obtained at 200°C, and recrysallization was usually observed starting from above 400°C. STO can be fully recrystallized at 700°C for very short time or 600° C for 5-15 minutes.

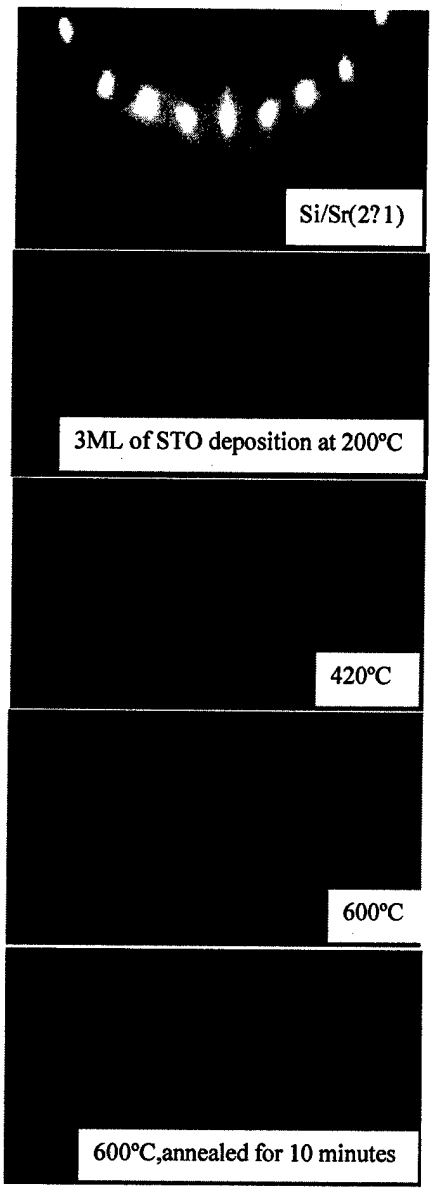


Fig. 3.8. The first cycle of recrystallization of 3 ML-thick STO 0n Si.

Figure 3.9 shows the RHEED patterns from STO after each cycle. The estimated total thickness of the STO was 5-10nm. The RHEED patterns have very narrow angular distrubtion of intensity, which indicates excellent crystallinity. The streaky pattern also indicate the STO surface is very smooth. A spotty pattern, however, also developed when the STO layer grew thicker, which indicates 3D islands began to form.

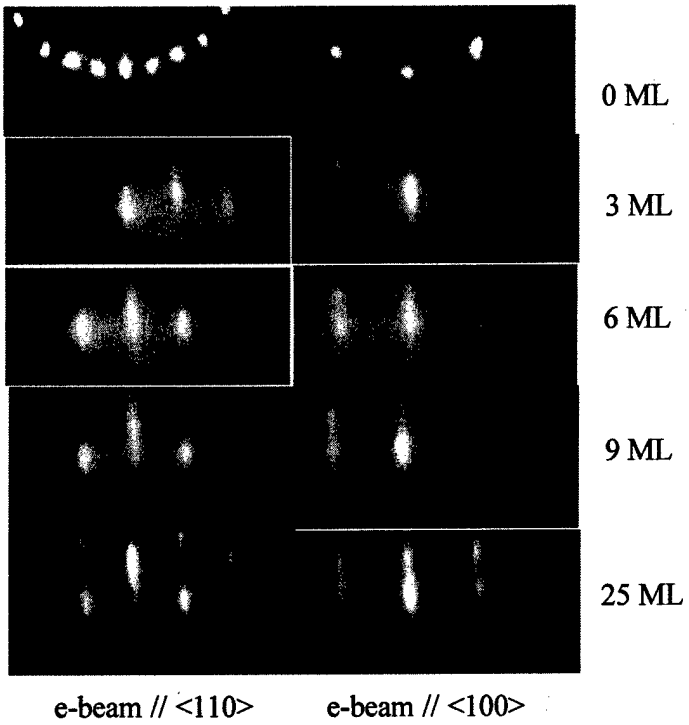


Fig. 3.9. RHEED patterns from STO film grown by multi-step recrystallization.

Figure 3.10 shows XRD scan taken from the STO/Si sample grown by multi-step recrystallization. In the figure, four diffraction peaks are visible and can be labeled as STO (001), Si (002), STO (002), Si (004). From this, the STO film grew epitaxially on Si with (001) STO // (001) Si. The full width at half maximum (FWHM) of STO (002) peak is 0.9 deg. Figure 3.11 shows thickness fringe of the STO/Si sample. From these fringes, the thickness of the STO layer is 33.9 Å.

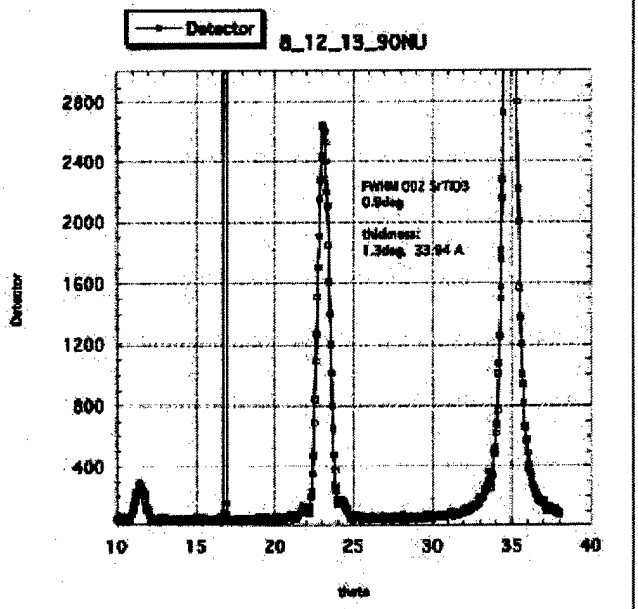


Fig. 3.10. XRD scan of an STO/Si sample grown by multi-step recrystallization.

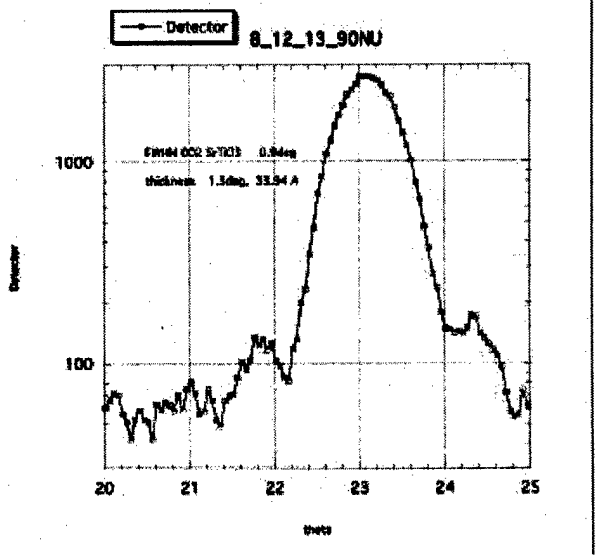


Fig. 3.11. Thickness fringes measured by X-ray reflectivity for the STO/Si sample grown by multi-step recrystallization. From the measurement, the thickness of the STO layer is 33.9 Å.

Figure 3.12 shows AFM images from STO surface grown by multi-step recrystallization. In some areas both 2D surface steps and small islands were observed, which presumably resulted from a combination of 2D and 3D growth. In some area many rectangular islands were observed with edges either parallel or perpendicular to Si<110> direction.This film had a refrative index of 2 as measured by ellipsometry.

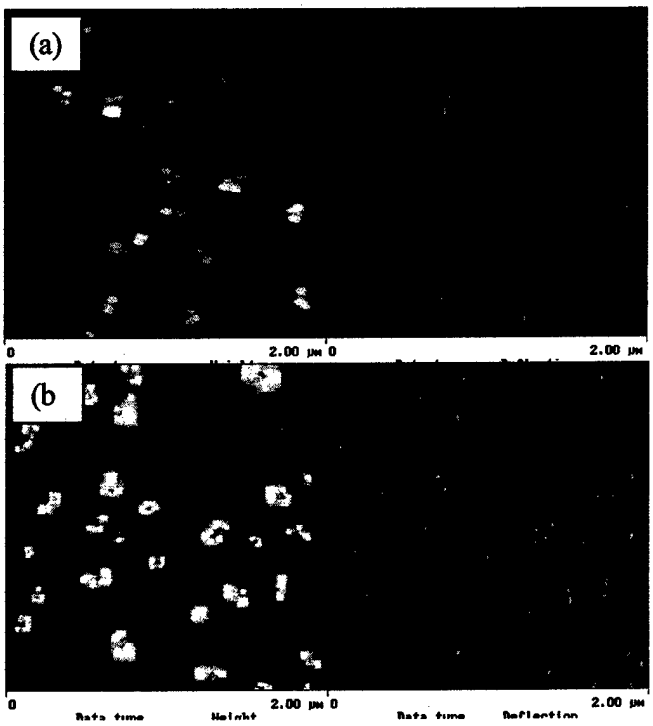


Fig. 3.12. AFM images taekn from STO grown at 200C? and recrystallized up to 600? for 4 cycles, total 32 minutes (Sr =375?C, Ti =1395?C), RMS roughness=3.2nm. (a) AFM image shows 2D steps and small islands, (b) AFM image shows rectangular islands in a different area.

Summary of Oxide Growth

RHEED analysis has indicated that the quality of the STO epitaxial layer grown under the optimal growth conditions using the solid-phase epitaxy process is close to phase pure and stoichiometric. The films are suitable for epitaxy of III-V compounds. However, further XPS and XRD analyses are needed to finely tune film compound stoichiometry since nonstoichiometry could introduce defects, amorphous and minor crystalline phases as well as increased thin film stress in STO.[1] Also surface morphology of STO layer might be further improved by lowering the recrystallization temperature and by fine tuning the STO stoichiometry to achieve 2D growth. Another potential approach is to grow thicker STO layers, while still keeping 2D growth mode. A relatively thicker STO layer is needed in order to act as an effective diffusion barrier for subsequent III-V semiconductor growth by MBE .

[1] T.Suzuki, Y.Nishi, and M.Fujimoto, Phil. Mag. A, 80(3), 621(2000).

4. InP Growth on Si

InP growth on MgO

The goal of this research program is to produce high quality single crystal InP layers on silicon substrates. InP and Si are both face centered cubic (FCC) crystals. However, InP has a lattice constant of 5.869 Å and Si has a lattice constant of 5.29 Å, a difference of 9.9%. Such a large difference in lattice sizes results in defects being created in the crystal during epitaxy and poor, unusable material quality. In addition, silicon is a non-polar homocrystal since it contains predominantly only one type of atom (Si). InP is a III-V compound semiconductor containing two atoms, In and P. Having two different atoms in the lattice creates polar fields. Growing polar InP on non-polar Si substrates leads to additional difficulty. Thus, an interfacial buffer layer is likely needed between the InP and Si.

One candidate explored for this interfacial layer is magnesium oxide (MgO). MgO is an oxide with an FCC lattice structure. Its lattice constant is 4.21 Å, which is greatly different than that of InP. However, if the epitaxial InP atoms were able to form in a lattice rotated 45° in the plane of the growth surface, the apparent lattice constant of the MgO could be seen as

$$\frac{4.21}{COS(45)} ? 5.95 \text{ Å}$$

which is close to the value of 5.869 Å for InP.

To test the viability of MgO as an interfacial layer, InP was grown in a solid source MBE system on bulk MgO substrate. The substrate was heated to 600 °C *in situ*, and the bare MgO surface was seen to be single crystal and smooth by the observation of diffraction lines on the RHEED surface analysis tool (Fig. 4.1). Approximately 3000 Å of InP was grown on this substrate at a temperature of 440 °C. A diffraction pattern on the RHEED analysis was not visible during the InP growth, indicating that the material was not likely to be of high quality. Room temperature photoluminescence (PL) of sample indicated InP was indeed grown, as seen by the spectral peak at ~ 950 nm in Fig. 4.2. However, the strength of the signal was very weak, indicating poor material quality.

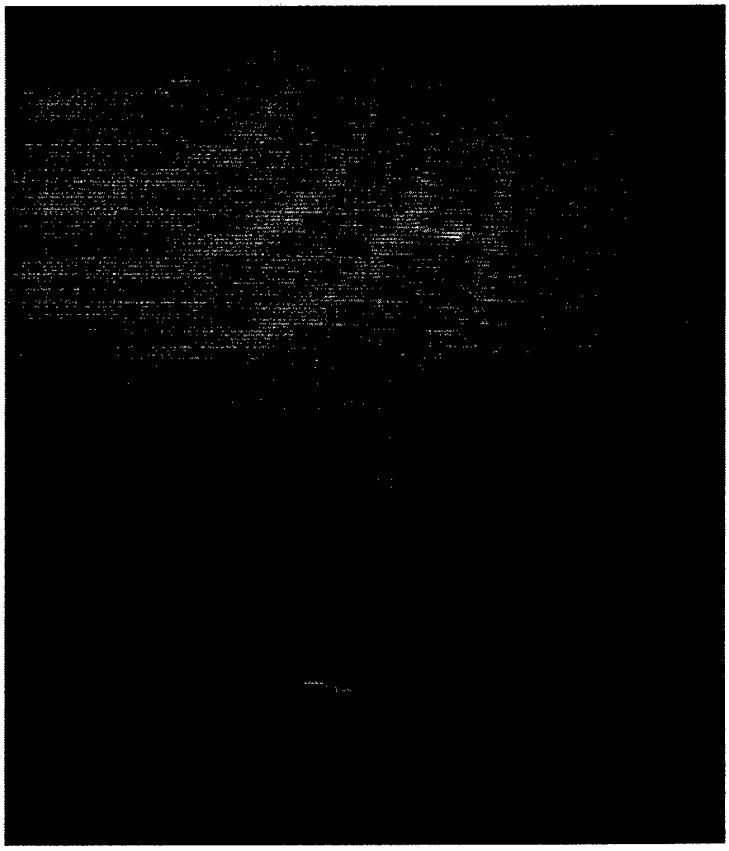


Figure 4.1

RHEED analysis of the bare MgO surface

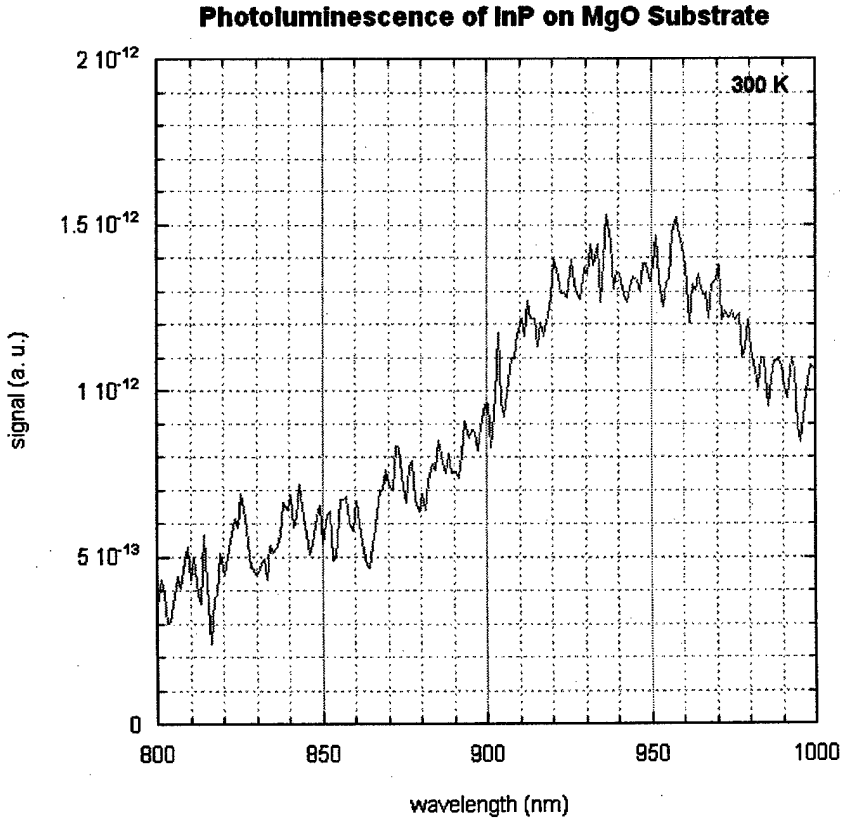


Figure 4.2

Room temperature photoluminescence (PL) of InP grown on MgO bulk substrate. The weak signal strength indicates low material quality.

The previous experiment confirmed that growth of InP on MgO was at least possible. A substrate was then obtained which consisted of bulk silicon with an epitaxial MgO grown on top. An InP layer was grown on top of this MgO/Si substrate. Room temperature PL spectra demonstrated a very weak InP signal (Fig. 4.3), material much lower in quality than the InP grown directly on bulk MgO substrate. From this data it was concluded that MgO was not a likely candidate to be the interfacial layer between Si and high-quality InP.

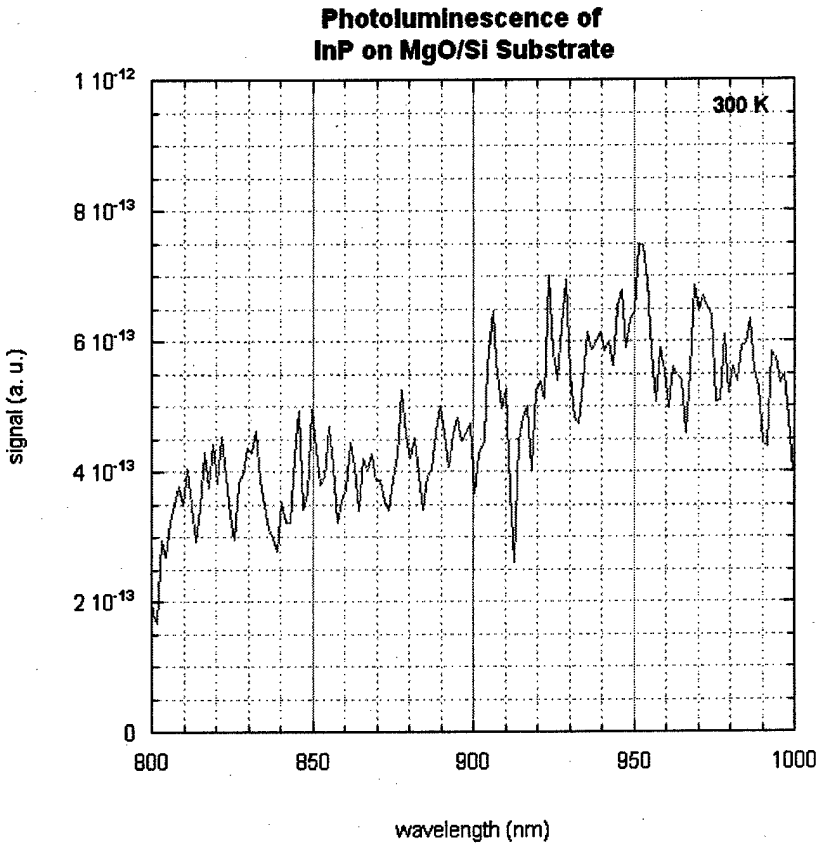


Figure 4.3. Room temperature PL of InP on silicon substrate with a MgO interfacial layer. The weak spectral signal is indicative of very poor InP quality.

InP Growth on Silicon-on-Insulator

A type of substrate commonly used in the silicon transistor industry is known as silicon-on-insulator (SOI). This type of material consists of a very thin layer of silicon bonded to a normal, thick bulk silicon wafer using an oxide (Fig. 4.4). Such a substrate is generally used for its electrically isolating properties. However, for the heteroepitaxy of InP on Si, the thin, isolated top layer of silicon offers the property of lattice compliancy. That is, the top Si layer is thin enough that it can change its lattice size to accommodate the strain of the InP growth. Bulk silicon substrate does not have this ability because it is large, massive and rigid. If the strain can

be absorbed by this thin Si layer instead of the epitaxially grown InP layer, the InP will have much reduced defects and be of higher quality. To this end, experimental InP growths were conducted on SOI substrates.

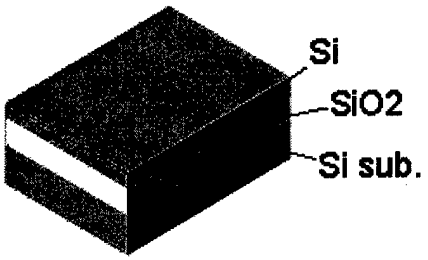


Figure 4.4 Diagram of silicon-on-insulator (SOI) substrates

SOI substrates were heated *in situ*, and a GaAs buffer layer was grown on top. This GaAs would serve as another intermediate transition layer since its lattice constant of 5.65 Å is between that of Si and InP. The first sample used a GaAs buffer layer thickness of 0.77 microns, on top of which 3500 Å of InP was grown. A weak InP signal was detected in the room temperature PL spectrum (Fig. 4.5).

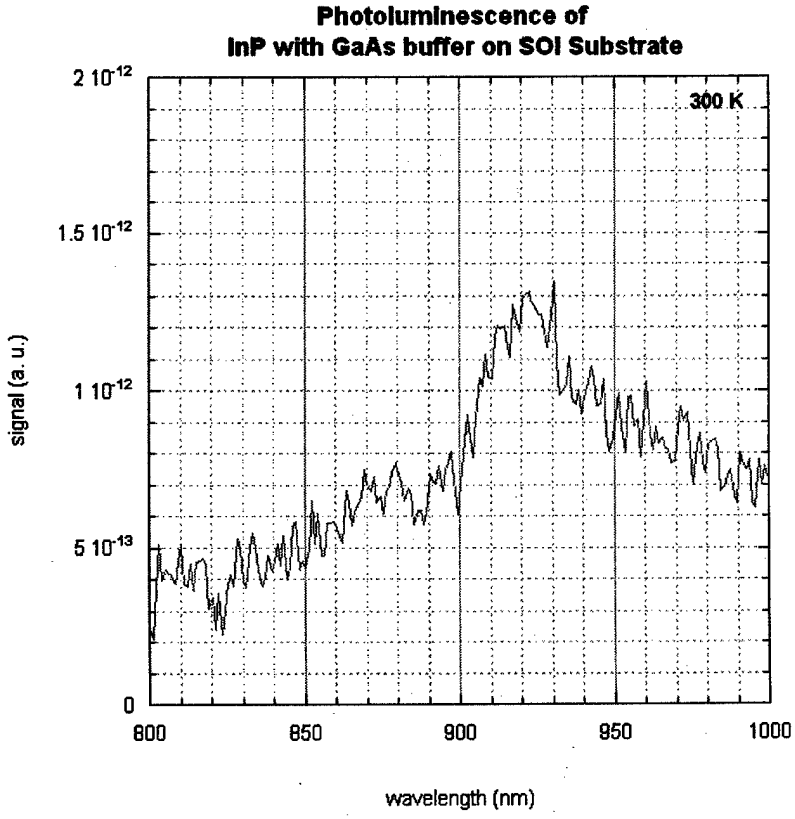


Figure 4.5

PL spectra of InP on SOI substrate with a 7700 Å GaAs buffer.

In another sample the GaAs buffer layer thickness was increased to 1.8 micron, and InP was again grown on top. Increasing this GaAs buffer did not improve the quality of the InP material (Fig. 4.6).

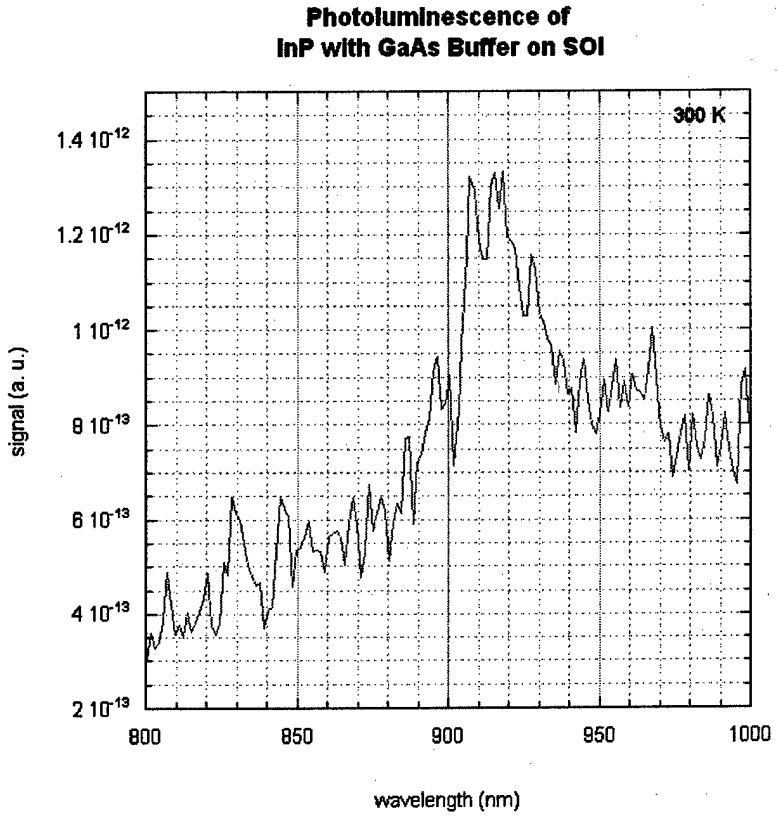


Figure 4.6 PL of InP on SOI substrate with an increased GaAs buffer thickness of 1.8 micron.

Using the GaAs buffer yielded marginal results. In an experiment, the buffer layer was changed to one using GaP and $In_xGa_{1-x}P$ layers. Gallium phosphide (GaP) has a lattice constant of 5.45 Å, which is close to that of silicon. It also serves well as a nucleation site interface between the non-polar silicon and polar III-V compounds. For this new buffer scheme, an initial layer of GaP was deposited, followed by four thin $In_xGa_{1-x}P$ layers, each with a different In/Ga composition ratio. The compositions changed from a gallium rich alloy, closest to the GaP layer, to an indium rich alloy just prior to the InP epilayer (Fig. 4.7). Again, this buffer was anticipated to provide additional strain relief, and thus a better InP growth.

InP	1 micron
$In_{0.65}Ga_{0.35}P$	150 Å
$In_{0.54}Ga_{0.46}P$	150 Å
$In_{0.30}Ga_{0.70}P$	150 Å
$In_{0.20}Ga_{0.80}P$	150 Å
GaP	400 Å
Silicon-on-Insulator	

Figure 4.7. Layer design of the InP on SOI growth using GaP/InGaP buffer layers.

Room temperature photoluminescence of the InP on SOI with a GaP/InGaP buffer reveals a much improved InP layer in that the spectral signal is much stronger (Fig. 4.8) than previously achieved. Even though the thickness of this GaP/InGaP buffer is much thinner than the GaAs buffer used previously, the resulting InP layer is far better.

SOI appears promising in achieving InP growth on large area silicon wafers. Currently the thickness of the isolated top Si layer is on the order of 1200 Å. In terms of strain relief, a thinner Si layer would perform better. However, creating extremely thin bonded Si layers is a challenge. This phase of the research shows that growing InP on thinner SOI layers is worth pursuing.

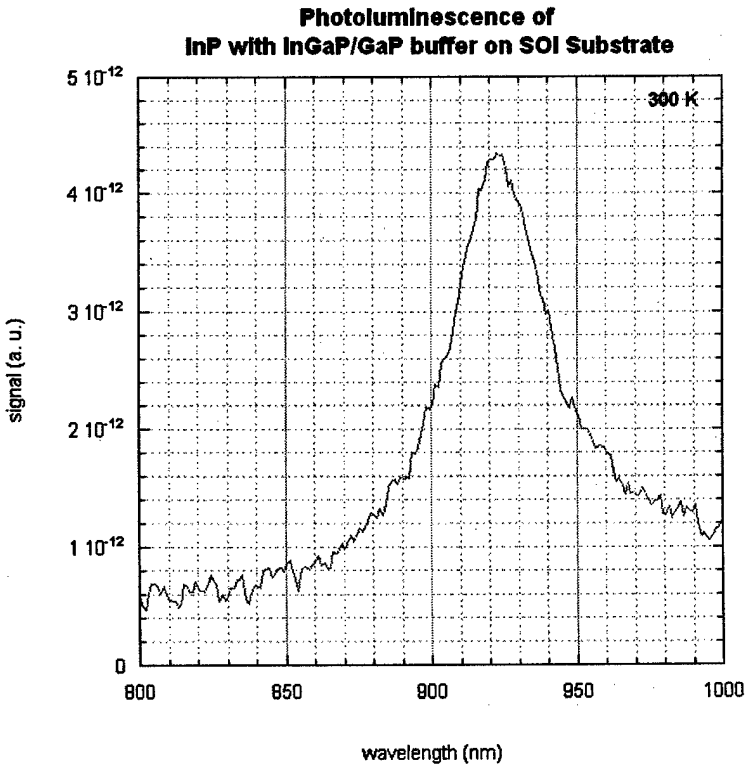


Figure 4.8

Room temperature PL of InP grown on SOI using a GaP/InGaP buffer layer sequence. The signal strength is indicative of good InP quality.

InP Growth on Strontium Titanate (STO)

Strontium titanate ($SrTiO_3$) is an oxide with a cubic lattice. Researchers at Motorola have previously demonstrated that STO can serve as a good interface layer to grow high quality GaAs on silicon wafers. As part of the Phase-I study in this report, the use of STO was applied to InP growth on silicon. Silicon wafers with epitaxially deposited STO were obtained from our research partners at Northwestern University as previously discussed. These wafers were loaded into the MBE system for InP growth.

For the first sample, InP was grown directly on the STO/Si wafer. InP was first deposited at a low temperature of 400 °C for the first 1500 Å of InP growth. The temperature was then raised to 460 °C for the remainder of the InP. No PL signal was observed for this sample however (Fig. 4.9). The poor material quality was attributable to either the direct deposition of InP (no buffer layer) or possibly insufficient phosphorus flux during growth. In the remaining samples, a buffer layer was introduced between the STO/Si and InP.

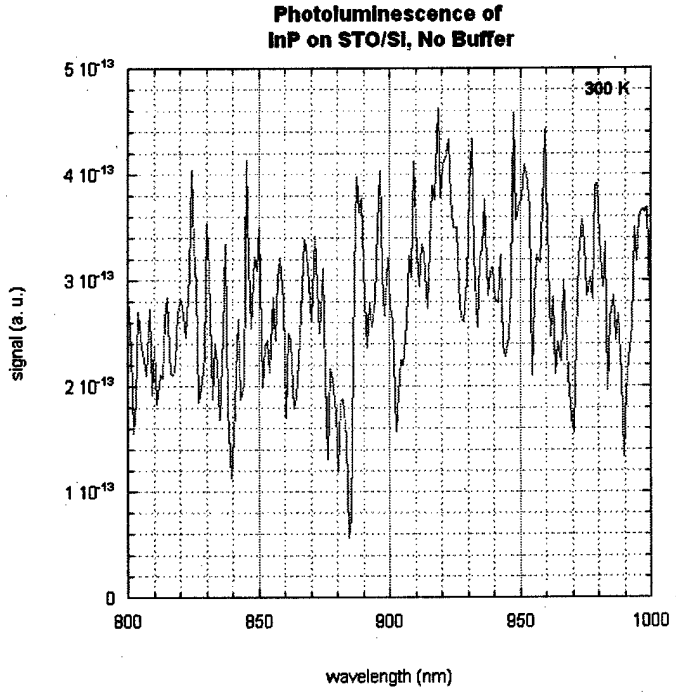
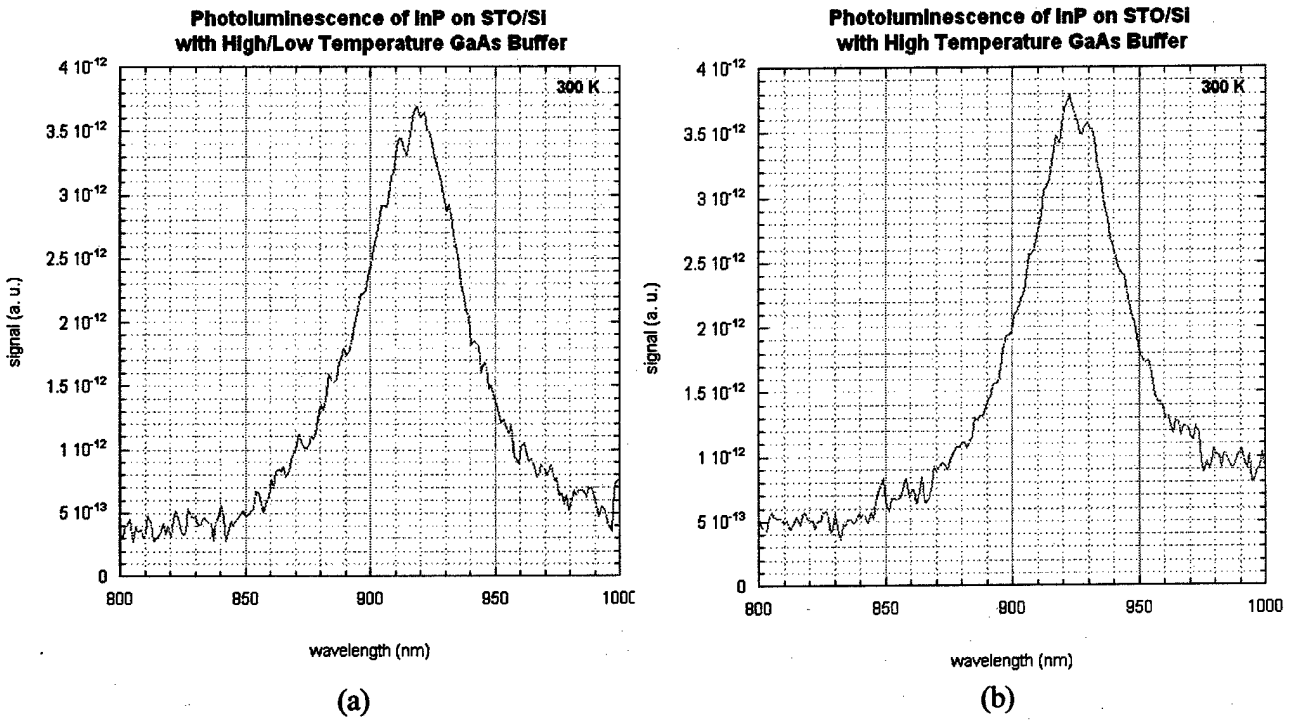


Figure 4.9. PL from InP directly grown on STO/Si (no buffer).

In succeeding samples, GaAs was used again as a buffer. The first of this series used GaAs layers grown at alternating high and low temperatures (560 and 400 °C, respectively), on top of an STO/Si wafer. Low temperature GaAs was thought to provide a strain relief, whereas high temperature provides better crystal quality. A total GaAs layer thickness of 1.8 micron was achieved, and InP was grown on top of this buffer. For a second sample, a thicker GaAs buffer of 2.4 microns was grown on the STO/Si, but all at a high temperature. 3500 Å of InP was then

deposited onto this buffer. Both of these samples yielded good PL spectra, comparable to one another (Fig. 4.10). The full width at half maximum (FHWM) value for these peaks were both ~ 45 nm. Compare this to an InP substrate wafer measured on the same PL system (Fig. 4.11). The FWHM for this bulk 350 micron thick InP crystal was 40 nm.



(a) (b)

Figure 4.10 PL spectra of InP on STO/Si wafers using a) low & high temperature GaAs buffer layer and b) high temperature buffer layer.

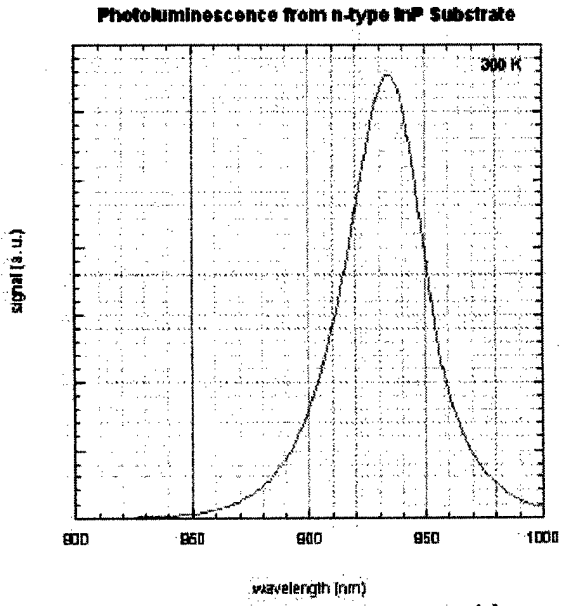


Figure 4.11

PL spectra of bulk InP substrate 350 microns thick.

These samples were also analyzed using x-ray diffraction. Diffraction data was first taken of bare STO on Si substrate to determine which peaks are from the STO/Si itself (Fig. 4.12). A sample of GaAs-only grown on STO/Si was measured to identify peaks due to GaAs growth (Fig. 4.13).

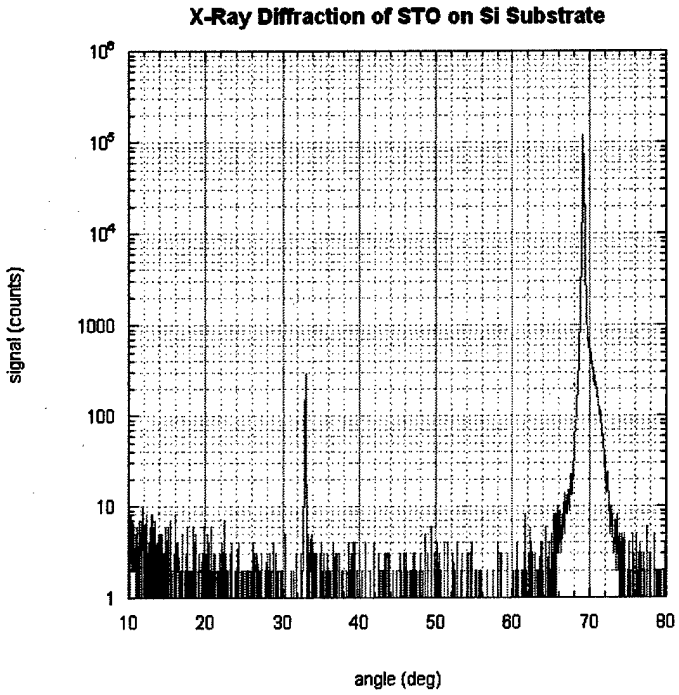


Figure 4.12

X-ray diffraction of bare STO on Si substrate

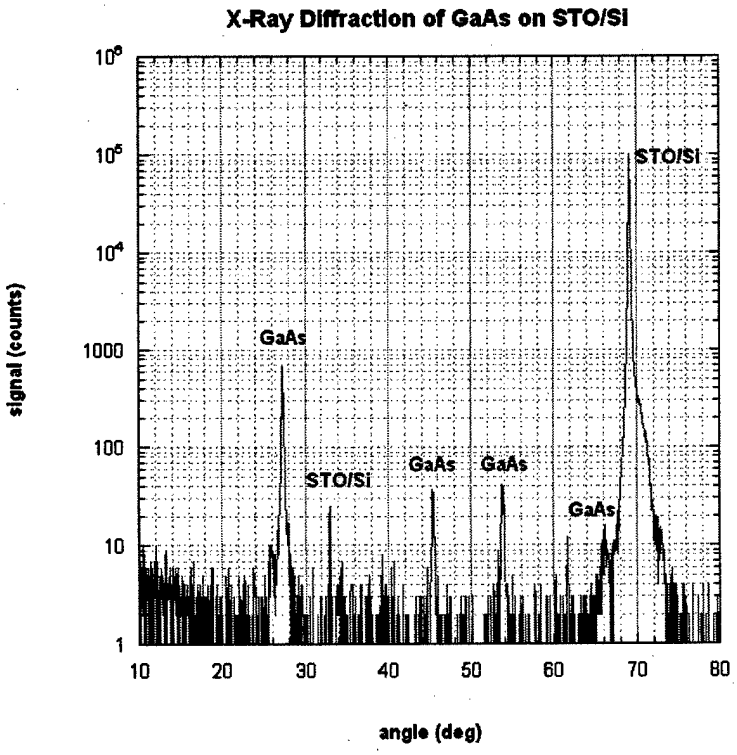


Figure 4.13

X-ray diffraction of GaAs grown on STO/Si substrate

X-ray of the two InP on STO/Si using GaAs buffer were compared (Fig. 4.14). Most evident are the relative magnitudes of the InP peaks. For the high/low temperature GaAs buffer scheme, the InP x-ray peak is only 50 counts per second. However for the high temperature only GaAs buffer, the resulting InP diffraction peak has a value of 2000. This data demonstrates how the buffer can greatly affect the crystalline quality of the final InP layer.

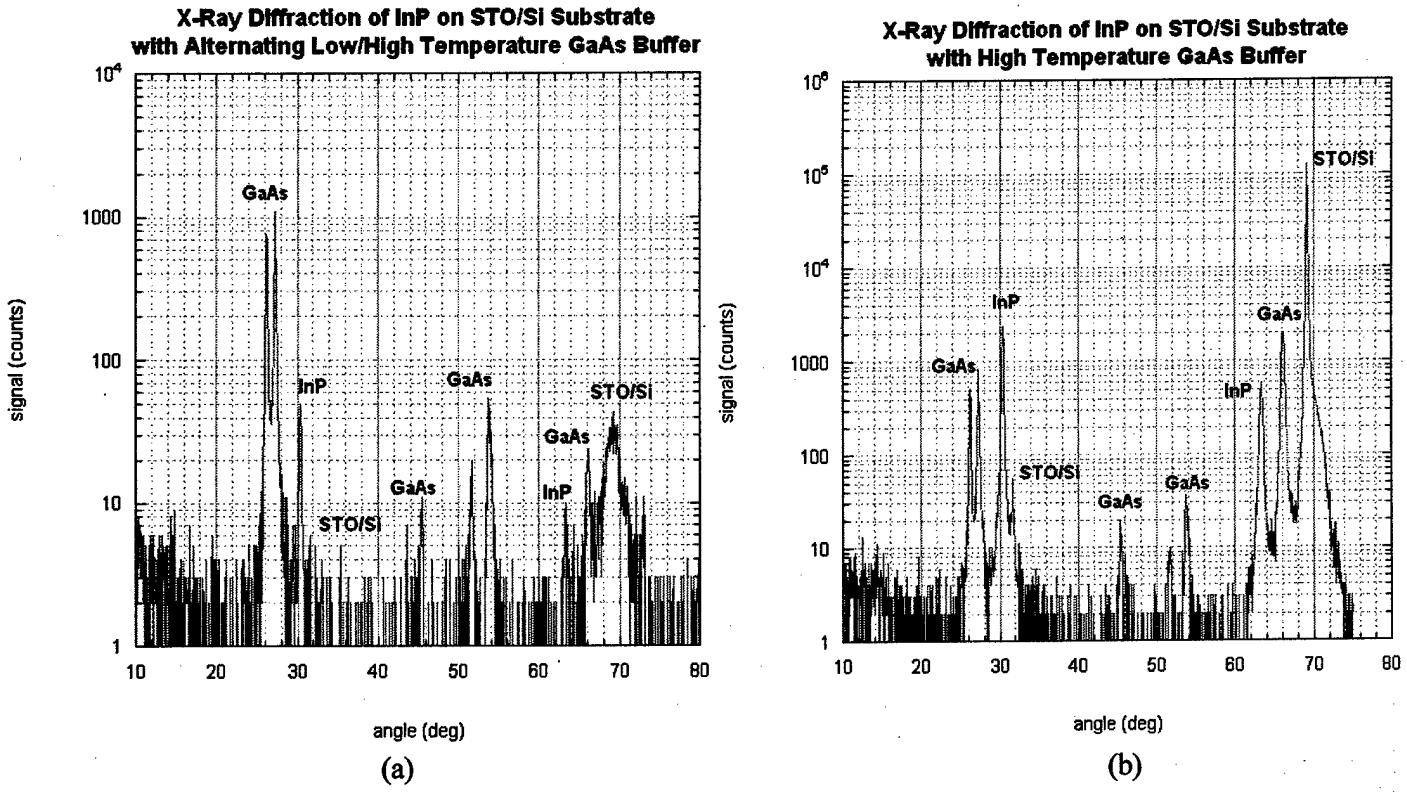


Figure 4.14. X-ray diffraction for the InP on STO/Si substrates with the a) high/low temperature GaAs buffer and b) high temperature only GaAs buffer.

A series of samples were grown on STO/Si using GaP buffer instead of GaAs. 500 Å of GaP was grown on the STO/Si substrates at a temperature of ~ 500 °C. 3500 Å of InP was then grown on top of these buffers at a growth temperature of 410, 450 or 500 °C. InP at the high and low ends of the growth temperature range weak PL signals (Fig. 4.15). For InP grown at 450 °C, the PL peak was strong (Fig. 4.16). In fact, the FHWM value for this spectral peak is 40 nm, the same value as that of the measured bulk InP substrate.

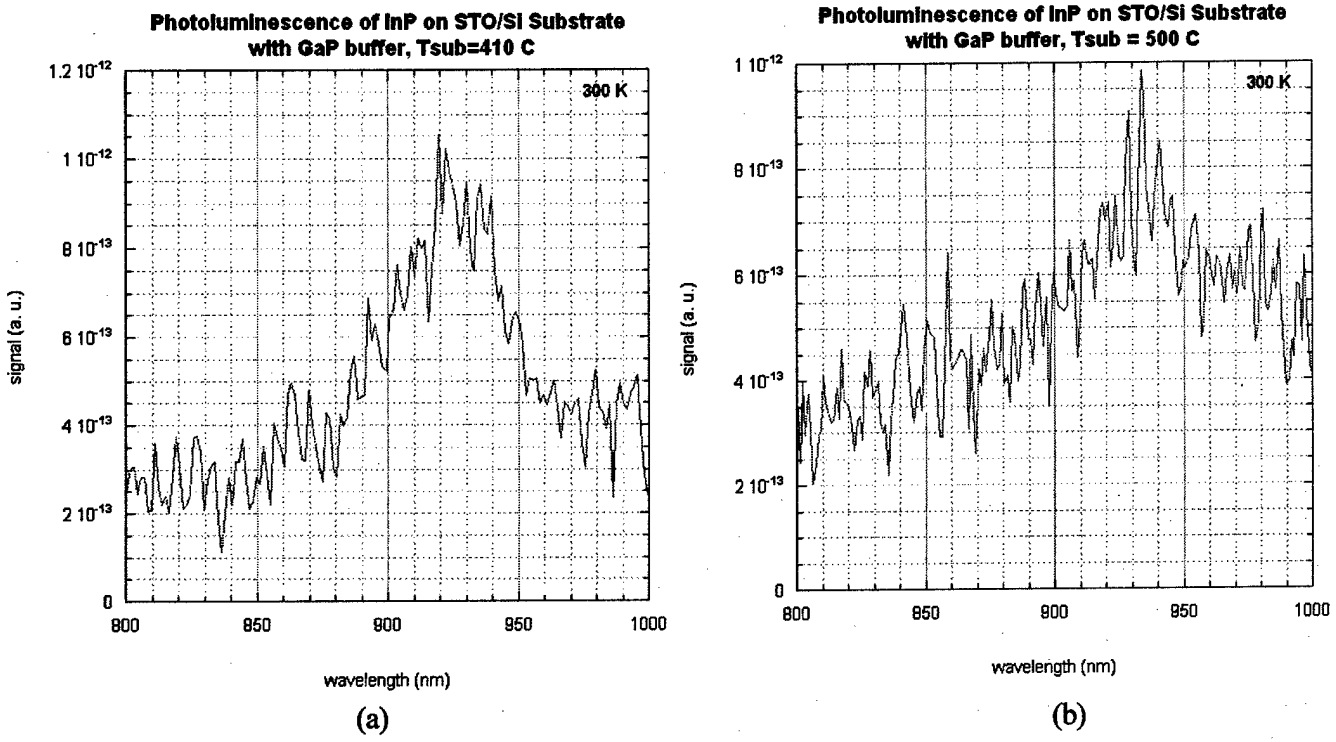


Figure 4.15 PL spectra from InP on STO/Si using a GaP buffer layer. The growth temperature during the InP layer was a) 410 and b) 500 °C.

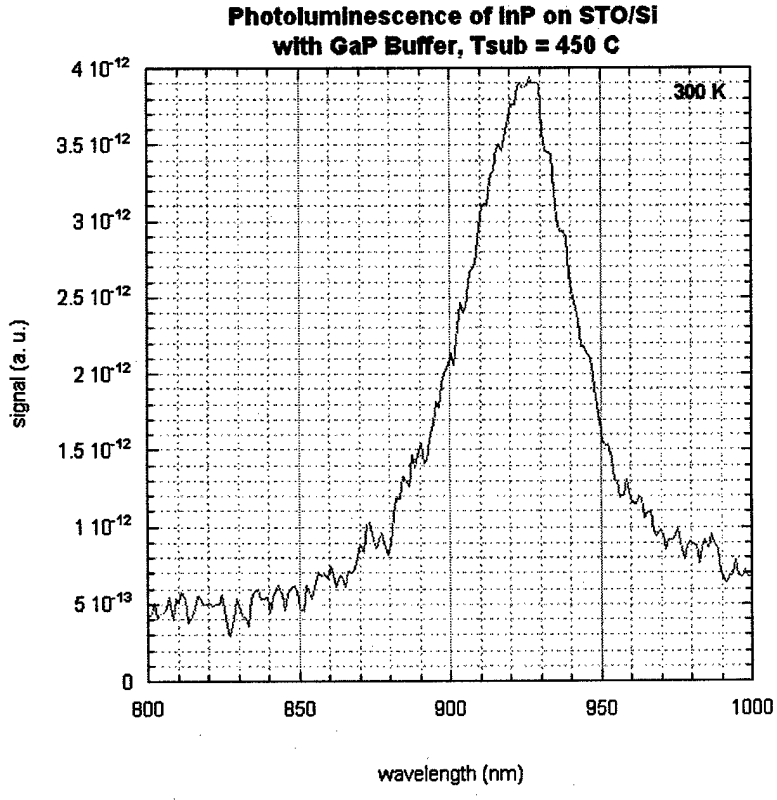


Figure 4.16

PL spectrum from InP on STO/Si grown at 450 °C using a GaP buffer.

X-ray diffraction data also supports the quality of this InP grown at 450 °C (Fig. 4.17). The signal for the InP peak was very strong at over 20,000 counts per second. This InP layer was measured electrically using the van der pau technique. The sample was n-type doped with Te. Room temperature hall mobility data indicated that the n-type doping concentration in this 3500 Å thick InP layer was $n=9x10^{18}$ cm^{-3} with a mobility of 746 $cm^2/V*sec$. In comparison, bulk InP at a doping level of $5x10^{17}$ cm^{-3} has a mobility of ~ 1500 $cm^2/V*sec$ at room temperature. Given the fact the grown InP on STO/Si layer here is very thin and at a higher doping level, the measured mobility value is another positive sign of the InP layer quality.

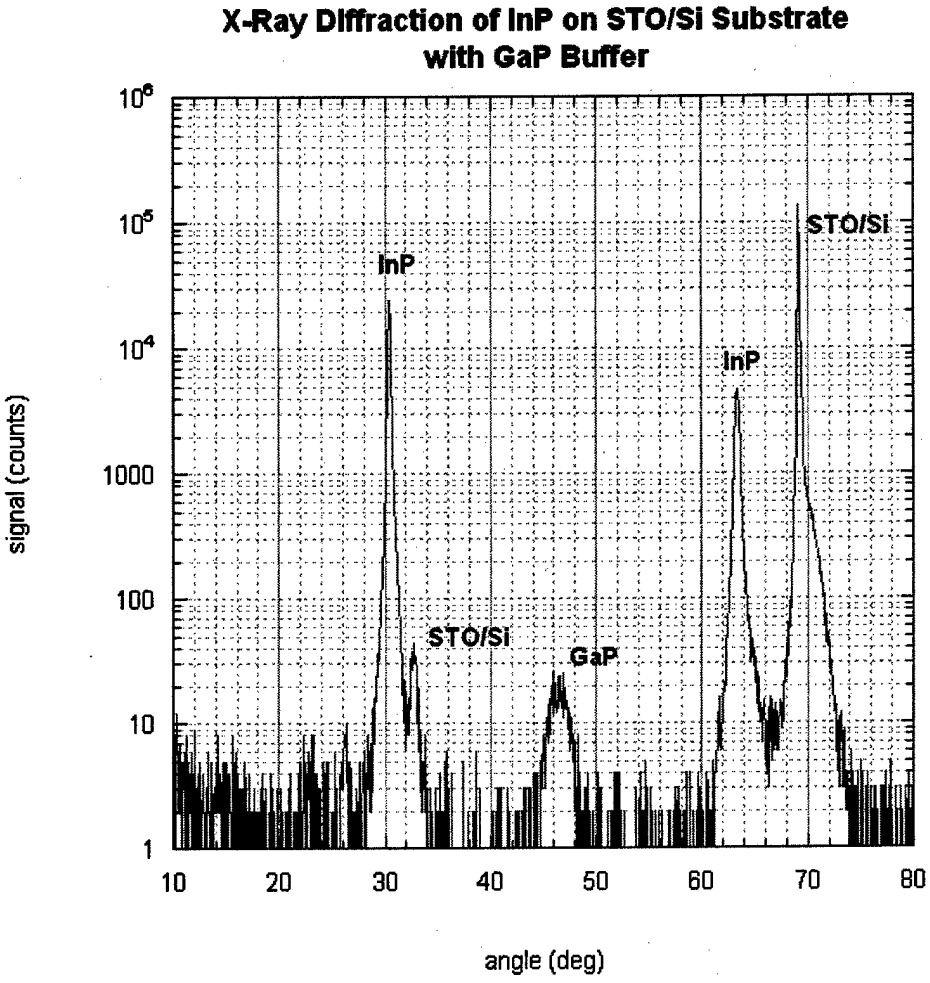


Figure 4.17 X-ray diffraction of InP grown on STO/Si at 450 °C using a GaP buffer layer.

5. Conclusion

This research program seeks to enable economical InP-based electronic devices. InP (indium phosphide) is a III-V compound semiconductor already in wide use today for such applications as high speed transistors, photodetectors and infrared lasers. The current hindrance to increased adoption of this technology is the relatively small size of InP substrate wafers, typically 3 inches diameter. In comparison, silicon electronics already employs 12 inch diameter wafers, and the size continues to increase. The result of this is that small wafers have less area for devices, increasing the cost or production per device unit.

In an effort to circumvent this substrate size issue, our research will ostensibly create InP wafers by depositing high quality, single crystal, thin films of InP onto large silicon wafers. A number of materials issues present obstacles to achieving this goal, such as lattice mismatch, anti-phase domains and thermal mismatches. Growing InP directly onto a silicon wafer currently results in unusable quality layers. An alternate approach is to use an interfacial layer between the silicon and InP. This layer would bridge the two dissimilar crystals such that the grown InP would be of high quality and have low defects.

This Phase I project successfully demonstrated that strontium titanate ($SrTiO_3$, a.k.a. STO) can serve as the critical interfacial layer between Si and InP. Our partners at Northwestern University developed a process to grow high quality films of STO on silicon. Using these wafers produced by Northwestern, we at SVT Associates applied our expertise in III-V epitaxy to grow InP layers on top of the STO/Si. Structural, electrical and optical characterization of this InP on silicon all provided evidence of the InP's good quality. Continuation onto the Phase II is highly warranted.

In the Phase II, Professor Wessels' group at Northwestern University will optimize their technique for producing epitaxial thin film oxides. Concurrently, SVT Associates will further improve the InP layers which are grown on these silicon wafers. Alternate buffer layer schemes will be explored to perfect the InP grown. Later in the Phase II, high speed InP-based devices will be fabricated and characterized onto these InP on Si substrates, as a demonstration of the commercial viability of this fabrication process.